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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/081,425	02/22/2002	Rajendra Pendse	CPAC 1011-2 US 9980			
22470	7590 08/09/2002					
	EFFEL & WOLFELD	EXAMINER				
	P O BOX 366 HALF MOON BAY, CA 94019			GEYER, SCOTT B		
			ART UNIT	PAPER NUMBER		
			2829			
		DATE MAIL ED: 08/09/2002				

Please find below and/or attached an Office communication concerning this application or proceeding.

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٠,		Application	on No.	Applicant(s)			
•		10/081,42	25	PENDSE, RAJEN	DRA		
	Office Action Summary	Examine	,	Art Unit			
		Scott B. G		2829			
	The MAILING DATE of this communi	cation appears on the	e cover sheet wit	h the correspondence ac	ddress		
Period for	REPITY REVELOE STATUTORY PERIOD FOR	AD DEDIVIS SET T	O EXPIRE 3 MC	NTH(S) FROM			
THE MA - Extensi after SI - If the pe - If NO p - Failure - Any rec	AILING DATE OF THIS COMMUNIONS of time may be available under the provisions of time may be available under the provisions of time may be available under the provisions of the commercial for reply specified above is less than thirty (30 period for reply is specified above, the maximum state to reply within the set or extended period for reply oly received by the Office later than three months at patent term adjustment. See 37 CFR 1.704(b).	CATION. of 37 CFR 1.136(a). In no evunication. or days, a reply within the state that the cause the angular by statute, cause the angular by statute.	rent, however, may a re tutory minimum of thirty vill expire SIX (6) MONT blication to become ABA	ply be timely filed (30) days will be considered time (HS from the mailing date of this of the control of the	ely. communication.		
1)⊠	Responsive to communication(s) file	ed on <u>08 July 2002</u> .					
,—	·	2b)⊠ This action is					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.							
-	n of Claims						
•	Claim(s) 1-11 is/are pending in the		cidoration				
	a) Of the above claim(s) <u>8-11</u> is/are	Withdrawn from con	sideration.				
•	Claim(s) is/are allowed.						
• —	☑ Claim(s) <u>1</u> is/are rejected.						
•	Claim(s) <u>2-7</u> is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement. Application Papers							
9)⊠ T	he specification is objected to by the	e Examiner.					
10)⊠ The drawing(s) filed on <u>13 May 2002</u> is/are: a)⊠ accepted or b) objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
11) 🗌 T	he proposed drawing correction file	d on is: a) 🗌	approved b)⊡ d	isapproved by the Exam	iner.		
If approved, corrected drawings are required in reply to this Office action.							
12) The oath or declaration is objected to by the Examiner.							
	nder 35 U.S.C. §§ 119 and 120	·					
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a)[All b) Some * c) None of:						
	1. Certified copies of the priority documents have been received.						
	2. Certified copies of the priority documents have been received in Application No.						
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 							
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).							
a) The translation of the foreign language provisional application has been received.							
15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.							
Attachment			A) 🗀 tatandani	Summary (PTO-413) Paper I	No(s)		
2) Notice	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (nation Disclosure Statement(s) (PTO-1449)	PTO-948) Paper No(s) <u>5</u> .	4)	Informal Patent Application (I	PTO-152)		

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DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-7, drawn to a method of encapsulating flip-chip interconnects, classified in class 438, subclass 107.
- II. Claims 8-11, drawn to an apparatus for applying a precise volume of encapsulating resin to an integrated circuit chip, classified in class 29, subclass 700+.

The inventions are distinct, each from the other because of the following reasons:

- **1A.** Inventions I and II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case, the apparatus could be used to apply resin to chips and dies other than those used in 'flip chip' bonding. Also, the apparatus recites a limitation for removing excess resin from a resin pool, a function unrelated to coating a chip with resin intended for bonding to a substrate.
- **1B.** Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

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1C. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

1D. During a telephone conversation with Bill Kennedy on August 2, 2002 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-7. Affirmation of this election must be made by applicant in replying to this Office action. Claims 8-11 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

1E. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Information Disclosure Statement

2. The references filed with the information disclosure statement, entered as paper no. 5, have been considered.

Drawings

3. The formal drawings, entered on 13 May 2002 as paper no. 4, are acceptable.

Specification

4. The disclosure is objected to because of the following informalities:

Page 3, line 15: change "features apparatus" to - - features an apparatus - -;

Page 3, line 15: change "applying precise" to - - applying a precise - -;

Page 3, line 21: change "measure volume" to - - measured volume - -;

Page 8, line 10: change "Also, apparatus" to - - Also, an apparatus - -.

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Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamaji (5,925,936).

As to claim 1, Yamaji teaches a method of encapsulating flip chip interconnects. A quantity of thermoplastic resin 3 is disposed upon the active side of a chip 5. The resin 3 surrounds the connection electrodes 4 as shown in figure 3A. After the resin 4 has been applied to the chip 5, the chip is bonded to a mounting substrate 6, wherein the connection electrodes 4 attach to substrate electrodes (bonding pads) 7.

(e) the invention was described in-

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7. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Witzman et al. (6,037,192).

As to claim 1, Witzman et al. teach a method of encapsulating flip chip interconnects, as shown in figures 3 and 4. In figure 3, a quantity of polymer adhesive

⁽¹⁾ an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

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(resin) 18 is applied to components (chips) 20. The adhesive is applied to the side of the components having interconnects 22. After the polymer adhesive 18 is applied to the components 20, the components 20 are bonded to substrates 10, wherein the substrates 10 possess conductors 12 and solderable pads (bonding pads) 16. The interconnects 22 of the component directly contact the solderable pads 16 to effect the electrical connection.

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8. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Chino et al. (6,184,066 B1).

As to claim 1, Chino et al. teach a method of encapsulating flip chip interconnects. The method, as described in column 1, lines 60-67 and continued to column 2, lines 1-8, includes applying a resin to either the semiconductor chip or the substrate to which the chip will be mounted.

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9. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Capote et al. (6,297,560 B1).

As to claim 1, Capote et al. teach a method of encapsulating flip chip interconnects. As shown in figure 4, solder bumps (interconnects) 14 on the active side of a chip 10 are coated in encapsulant material (resin) 22. After the application of the encapsulant 22, the chip 10 is bonded to a substrate 20, such that the solder bumps 14 of the chip 10 electrically connect to solder pads (bonding pads) 12 of the substrate 20.

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Allowable Subject Matter

10. Claims 2-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Ball (6,097,098), Gilleo et al. (6,323,062 B1) and Kirsten (6,367,150 B1) are cited which teach similar dipping methods. Ball teaches dipping a completed device in a epoxy or silicon gel to apply a protective coating (column 5, lines 60 et seq.). Gilleo et al. teach a method of dipping the bumps, which are attached to the underside of a chip, into a flux so as to coat the bumps with flux prior to mounting the chip to a substrate (column 5, lines 18-35). Kirsten also teaches a method of dipping a chip, with solder bumps, into a flux so as to coat the solder bumps with flux. After the flux has been coated onto the solder bumps, the chip is bonded to a substrate. After the chip has been attached to the substrate, encapsulant is introduced into the gap between the substrate and chip (column 5, lines 55 et seq.).

The prior art of record, and to the examiner's knowledge, does not teach or render obvious at least to the skilled artisan the instant invention regarding, in a first limitation a step of applying resin to a chip by dipping the interconnect side of the chip to a predetermined depth into a pool of resin, and in a second limitation a step of applying a resin to a chip by dipping the interconnect side of the chip into a reservoir of resin to a predetermined depth wherein the bumps on the interconnect side of the chip contact the bottom of the reservoir.

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Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (703) 306-5866. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm. The examiner may also be reached via e-mail: scott.geyer@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Sherry can be reached on (703) 308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SBG August 7, 2002 VINH P. NGUYEN PRIMARY EXAMINER GROUP 2829

08/07/2002